

# 1.5 Amp Output Current IGBT Gate Driver Optocoupler

# with Integrated ( $V_{CE}$ ) Desaturation Detection, UVLO Fault Status Feedback, Active Miller Clamping

# Description

The SJS-331J is an advanced 1.5 A output current, easy-to-use, intelligent gate driver which makes IGBT  $V_{CE}$  fault protection compact, affordable, and easy-to implement. Features such as integrated  $V_{CE}$  detection, under voltage lockout (UVLO), "soft" IGBT turn-off, isolated open collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

The SJS-331J contains a LED. The LED is optically coupled to an integrated circuit with a power output stage. SJS-331J is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 100 A.

For IGBTs with higher ratings, the SJS-331J can be used to drive a discrete power stage which drives the IGBT gate.

The SJS-331J has an insulation voltage of V<sub>IORM</sub> = 1414 V<sub>PEAK</sub>.

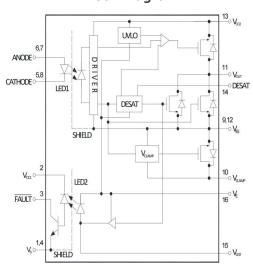
#### **Features**

- 1.5 A maximum peak output current
- 1.0 A minimum peak output current
- 250 ns maximum propagation delay over temperature range
- 1.0 A Active Miller Clamp. Clamp pin short to V<sub>EE</sub> if not in used
- Miller Clamping
- Desaturation Detection
- Under Voltage Lock-Out Protection (UVLO) with Hysteresis
- "Soft" IGBT Turn-off
- Fault Reset by next LED turn-on (low to high) after fault mute period
- Available in SO-16 package
- 100 ns maximum pulse width distortion (PWD)
- 50 kV/ $\mu$ s minimum common mode rejection (CMR) at  $V_{CM} = 1500 \text{ V}$
- I<sub>CC</sub> (max) < 5 mA maximum supply current
- Wide  $V_{cc}$  operating range: 15 V to 30 V over temperature range
- Wide operating temperature range: -40°C to 110°C

#### **Applications**

- Isolated IGBT/Power MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters and Uninterruptible Power Supply (UPS)

# **Block Diagram**





SCHEMATIC	PIN DEFINITION			
1	1. V <sub>S</sub> 16. V <sub>E</sub> 2. V <sub>CC1</sub> 15. V <sub>LED</sub> 3. FAULT 14. DESAT 4. V <sub>S</sub> 13. V <sub>CC2</sub> 5. CATHODE 12. V <sub>EE</sub> 6. ANODE 11. V <sub>OUT</sub> 7. ANODE 10. V <sub>CLAMP</sub>			
8 CATHODE V <sub>EE</sub> 9	8. CATHODE 9. V <sub>EE</sub>			

ABSOLUTE MAXIMUM RATINGS								
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	Note			
Storage Temperature	Tstg	-55	125	°C				
Operating Temperature	T <sub>A</sub>	-40	110	°C	2			
Output IC Junction Temperature	Tı		125	°C	2			
Average Forward Input Current	IF		25	mA	1			
Peak Transient Input Current (<1 μs pulse width, 300pps)	I <sub>F(TRAN)</sub>		1.0	А				
Reverse Input Voltage	V <sub>R</sub>		5	V				
"High" Peak Output Current	I <sub>OH(PEAK)</sub>		1.5	А	3			
"Low" Peak Output Current	I <sub>OL(PEAK)</sub>		1.5	А	3			
Positive Input Supply Voltage	V <sub>CC1</sub>	-0.5	7.0	V				
FAULT Output Current	I <sub>FAULT</sub>		8.0	mA				
FAULT Pin Voltage	V <sub>FAULT</sub>	-0.5	V <sub>CC1</sub>	V				
Total Output Supply Voltage	(V <sub>CC2</sub> - V <sub>EE</sub> )	-0.5	33	V				
Negative Output Supply Voltage	(V <sub>E</sub> - V <sub>EE</sub> )	-0.5	15	V	6			
Positive Output Supply Voltage	(V <sub>CC2</sub> - V <sub>E</sub> )	-0.5	33-(V <sub>E</sub> -V <sub>EE</sub> )	V				
Gate Drive Output Voltage	V <sub>O(PEAK)</sub>	-0.5	V <sub>CC2</sub>	V				
Peak Clamping Sinking Current	I <sub>Clamp</sub>		1.0	А				
Miller Clamping Pin Voltage	V <sub>Clamp</sub>	-0.5	V <sub>CC2</sub>	V				
DESAT Voltage	V <sub>DESAT</sub>	V <sub>E</sub>	V <sub>E</sub> +10	V				
Output IC Power Dissipation	Po		600	mW	2			
Input IC Power Dissipation	Pı		150	mW	2			
Solder Reflow Temperature Profile		See	Package Outline Drav	vings section				



RECOMMENDED OPERATION CONDITIONS									
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	Note				
Operating Temperature	T <sub>A</sub>	-40	110	°C	2				
Total Output Supply Voltage	(V <sub>CC2</sub> - V <sub>EE</sub> )	15	30	V	7				
Negative Output Supply Voltage	(V <sub>E</sub> - V <sub>EE</sub> )	0	15	V	4				
Positive Output Supply Voltage	(V <sub>CC2</sub> - V <sub>E</sub> )	15	30-(V <sub>E</sub> -V <sub>EE</sub> )	V					
Input Current (ON)	I <sub>F(ON)</sub>	8	12	mA					
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V					

	ELECTRICAL OPTICAL CHARACTERISTICS								
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note		
		INPUT (	CHARACTE	RISTICS		•			
	.,		0.01	0.4	V	I <sub>FAULT</sub> = 1.1 mA, V <sub>CC1</sub> = 5.5V			
FAULT Logic Low Output Voltage	V <sub>FAULTL</sub>		0.02	0.4	V	I <sub>FAULT</sub> = 1.1 mA, V <sub>CC1</sub> = 3.3V			
FALLET Lawis Likely Outhout Command			0.01	0.5	μΑ	V <sub>FAULT</sub> = 5.5 V, V <sub>CC1</sub> = 5.5V			
FAULT Logic High Output Current	I <sub>FAULTH</sub>		0.006	0.3	μΑ	V <sub>FAULT</sub> = 3.3 V, V <sub>CC1</sub> = 3.3V			
High Loyal Output Current		-0.3	-1		А	$V_0 = V_{CC2} - 4$	5		
High Level Output Current	I <sub>OH</sub>	-1.0			А	$V_0 = V_{CC2} - 15$	3		
Law Laval Outrot Compat		0.3	1		А	V <sub>O</sub> = V <sub>EE</sub> + 2.5	5		
Low Level Output Current	I <sub>OL</sub>	1.0			А	V <sub>O</sub> = V <sub>EE</sub> + 15	3		
Low Level Output Current During Fault Condition	I <sub>OLF</sub>	70	110	230	mA	V <sub>OUT</sub> - V <sub>EE</sub> = 14 V	6		
High Level Output Voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.5	V <sub>CC</sub> -0.1		V	Ι <sub>O</sub> = -650 μΑ	7,8,9,23		
Low Level Output Voltage	V <sub>OL</sub>		0.1	0.5	V	I <sub>O</sub> = 100 mA			
Clamp Pin Threshold Voltage	$V_{tClamp}$		2.2		V				
Clamp Low Level Sinking Current	I <sub>CL</sub>	0.21	0.8		А	V <sub>O</sub> = V <sub>EE</sub> + 2.5			
High Level Supply Current	І <sub>сс2Н</sub>		2.23	5	mA	I <sub>O</sub> = 0 mA	9		
Low Level Supply Current	I <sub>CC2L</sub>		2.36	5	mA	I <sub>O</sub> = 0 mA			
Blanking Capacitor Charging Current	I <sub>CHG</sub>	0.13	-0.24	-0.33	mA	V <sub>DESAT</sub> = 2 V	9,10		
Blanking Capacitor Discharge Current	I <sub>DSCHG</sub>	10	31		mA	V <sub>DESAT</sub> = 7.0 V			
DESAT Threshold	$V_{DESAT}$	6	6.7	7.5	V	V <sub>CC2</sub> -V <sub>E</sub> >V <sub>UVLO</sub> -	9		
IN ( O There should	V <sub>UVLO+</sub>	10.5	11.5	12.5	V	V <sub>0</sub> > 5 V	7,9,11		
UVLO Threshold	V <sub>UVLO</sub> -	9.2	10.5	11.1	V	V <sub>0</sub> < 5 V	7,9,12		
UVLO Hysteresis	(V <sub>UVLO+</sub> - V <sub>UVLO-</sub> )	0.4	1		V				
Threshold Input Current Low to High	I <sub>FLH</sub>		0.27	6	mA	I <sub>O</sub> = 0 mA, V <sub>O</sub> > 5 V			
Threshold Input Voltage High to Low	$V_{FHL}$	0.8	1.74		V				



Input Forward Voltage	V <sub>F</sub>	1.6	2.0	2.4	V	I <sub>F</sub> = 10 mA	
Input Reverse Breakdown Voltage	$BV_R$	5			V	Ι <sub>R</sub> = 10 μΑ	
Input Capacitance	C <sub>IN</sub>		70		рF	f = 1 MHz, V <sub>F</sub> = 0 V	

■ Unless otherwise noted, all typical values at  $T_A = 25$ °C,  $V_{CC2} - V_{EE} = 30$  V,  $V_E - V_{EE} = 0$  V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

	SI	NITCHIN	IG SPEC	IFICATIO	N		
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note
	:	SWITCHIN	G CHARA	CTERISTICS	5		
Propagation Delay Time to Output Low Level	t <sub>PHL</sub>	50	103	250	ns		
Propagation Delay Time to Output High Level	t <sub>PLH</sub>	50	74	250	ns	Rg = 20 Ω, Cg = 5 nF,	13,15
Pulse Width Distortion	PWD	-100		100	ns	f = 10 kHz, Duty Cycle = 50%,	14,17
Propagation Delay Difference Between Any Two Parts	PDD (t <sub>PHL</sub> - t <sub>PLH</sub> )	-150		150	ns	I <sub>F</sub> = 10 mA, V <sub>CC2</sub> = 30 V	17,16
Rise Time	t <sub>r</sub>		45		ns		
Fall Time	t <sub>f</sub>		40		ns		
DESAT Sense to 90% VO Delay	t <sub>DESAT(90%)</sub>		0.1	0.3	μs	$C_{DESAT}$ = 100 pF, $R_F$ = 2.1k $\Omega$ , $Rg$ = 20 $\Omega$ , $Cg$ = 5 nF, $V_{CC2}$ = 30 V	19
DESAT Sense to 10% VO Delay	t <sub>DESAT(10%)</sub>		1.2	1.5	μs	$C_{DESAT}$ = 100 pF, $R_F$ = 2.1k $\Omega$ , $Rg$ = 20 $\Omega$ , $Cg$ = 5 nF, $V_{CC2}$ = 30 V	
DESAT Sense to Low Level FAULT			0.15	0.5	μs	$C_{DESAT}$ = 100 pF, $R_F$ = 2.1k $\Omega$ , $C_F$ = Open, $Rg$ = 20 $\Omega$ , $Cg$ = 5 nF, $V_{CC2}$ = 30 V	40
Signal Delay	t <sub>DESAT(FAULT)</sub>		0.8		μs	$C_{DESAT} = 100 \text{ pF}, R_F = 2.1 \text{k}\Omega,$ $C_F = 1 \text{ nF}, Rg = 20 \Omega,$ $Cg = 5 \text{ nF}, V_{CC2} = 30 \text{ V}$	18
DESAT Sense to DESAT Low Propagation Delay	t <sub>DESAT(LOW)</sub>		0.1		μs	$C_{DESAT}$ = 100 pF, $R_F$ = 2.1k $\Omega$ , $Rg$ = 20 $\Omega$ , $Cg$ = 5 nF, $V_{CC2}$ = 30 V	19
DESAT Input Mute	t <sub>DESAT</sub> (MUTE)	5			μs	$C_{DESAT} = 100 \text{ pF}, R_F = 2.1 \text{k}\Omega,$ $Rg = 20 \Omega, Cg = 5 \text{ nF},$ $V_{CC1} = 5.5 \text{V}, V_{CC2} = 30 \text{ V}$	20



RESET to High Level FAULT	treset(fault)	0.2	0.6	2.0	μs	$C_{DESAT} = 100 \text{ pF, RF} = 2.1 \text{ k}\Omega,$ $Rg = 20 \Omega, Cg = 5 \text{ nF,}$ $V_{CC1} = 5.5 \text{V}, V_{CC2} = 30 \text{ V}$	
Signal Delay	t <sub>RESET(FAULT)</sub>	0.2	0.6	2.0	μs	$C_{DESAT} = 100 \text{ pF, RF} = 2.1 \text{ k}\Omega,$ $Rg = 20 \Omega, Cg = 5 \text{ nF,}$ $V_{CC1} = 3.3 \text{V}, V_{CC2} = 30 \text{ V}$	
Output High Level Common Mode Transient Immunity	CM <sub>H</sub>	15			· kV/μs	$T_A = 25$ °C, $I_F = 10$ mA $V_{CM} = 1500$ V, $V_{CC2} = 30$ V, $R_F = 2.1$ k $\Omega$ , $C_F = 15$ pF $T_A = 25$ °C, $I_F = 10$ mA	21
		50				$V_{CM} = 1500 \text{ V}, V_{CC2} = 30 \text{ V},$ $R_F = 2.1 \text{ k}\Omega, C_F = 1 \text{ n}F$	21,26
Output Low Level Common	ICM I	15			kV/μs	$T_A = 25$ °C, $V_F = 0$ V $V_{CM} = 1500$ V, $V_{CC2} = 30$ V, $V_{CC2} = 15$ pF	22
Mode Transient Immunity	CM <sub>L</sub>	50				$T_A = 25^{\circ}\text{C}, V_F = 0 \text{ V}$ $V_{CM} = 1500 \text{ V}, V_{CC2} = 30 \text{ V},$ $R_F = 2.1 \text{ k}\Omega, C_F = 1 \text{ nF}$	

■ Unless otherwise noted, all typical values at  $T_A = 25$ °C,  $V_{CC2} - V_{EE} = 30$  V,  $V_E - V_{EE} = 0$  V; all Minimum/Maximum specifications are at Recommended Operating Conditions.

ISOLATION CHARACTERISTIC									
PARAMETER	SYMBOL	DEVICE	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note	
Withstand Insulation Test Voltage	V <sub>ISO</sub>	SJS-331J	5000	-	-	V	RH $\leq$ 40%-60%, t = 1min, T <sub>A</sub> = 25 °C	24,25	
Input-Output Resistance	R <sub>I-O</sub>	-	1	1012	1	Ω	V <sub>I-O</sub> = 500V DC	25	

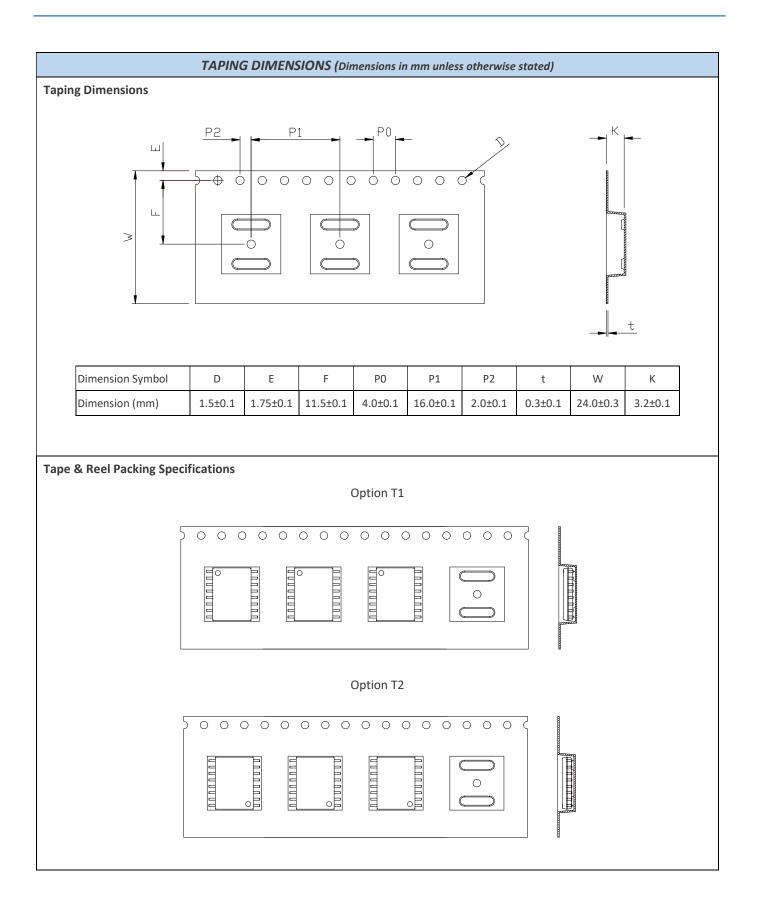
#### Notes:

- 1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
- 2. In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at 10 mW/°C above 90°C. Input IC power dissipation does not require derating.
- 3. Maximum pulse width =  $10 \mu s$ . This value is intended to allow for component tolerances for designs with IO peak minimum = 1.0 A. Derate linearly from 2.0 A at +25 °C to 1.5 A at +105 °C. This compensates for increased  $I_{OPEAK}$  due to changes in  $V_{OL}$  over temperature.

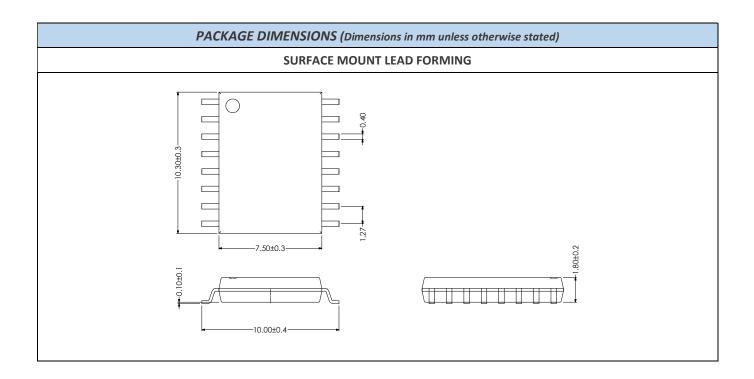


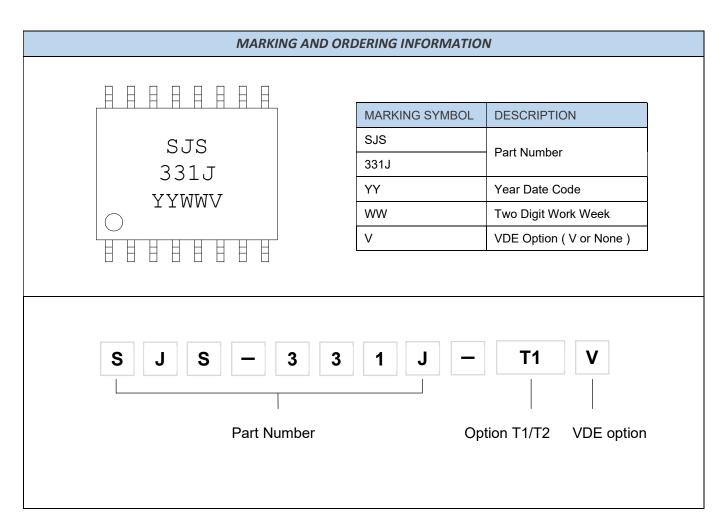
- 4. This supply is optional. Required only when negative gate drive is implemented.
- 5. Maximum pulse width =  $50 \mu s$ .
- 6. See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.
- 7. 15 V is the recommended minimum operating positive supply voltage (V<sub>CC2</sub> V<sub>E</sub>) to ensure adequate margin in excess of the maximum V<sub>UVLO+</sub> threshold of 12.5 V. For High Level Output Voltage testing, V<sub>OH</sub> is measured with a dc load current. When driving capacitive loads, V<sub>OH</sub> will approach V<sub>CC</sub> as I<sub>OH</sub> approaches zero units.
- 8. Maximum pulse width = 1.0 ms.
- 9. Once VO of the SJS-331J is allowed to go high (Vcc2 VE > VUVLO+), the DESAT detection feature of the SJS-331J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once Vcc2 is increased from 0V to above VUVLO+, DESAT will remain functional until Vcc2 is decreased below VUVLO-. Thus, the DESAT detection and UVLO features of the SJS-331J work in conjunction to ensure constant IGBT protection.
- 10. See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
- 11. This is the "increasing" (i.e. turn-on or "positive going" direction) of  $V_{CC2} V_E$
- 12. This is the "decreasing" (i.e. turn-off or "negative going" direction) of  $V_{CC2} V_E$
- 13. This load condition approximates the gate load of a 1200 V/75A IGBT.
- 14. Pulse Width Distortion (PWD) is defined as | tphl tplh | for any given unit.
- 15. As measured from  $I_F$  to  $V_O$ .
- 16. The difference between t<sub>PHL</sub> and t<sub>PLH</sub> between any two SJS-331J parts under the same test conditions.
- 17. As measured from ANODE, CATHODE of LED to Vout
- 18. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
- 19. This is the amount of time the DESAT threshold must be exceeded before V<sub>OUT</sub> begins to go low, and the FAULT output to go low. This is supply voltage dependent.
- 20. Auto Reset: This is the amount of time when V<sub>OUT</sub> will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
- 21. Common mode transient immunity in the high state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (i.e.,  $V_O > 15$  V or FAULT > 2 V).
- 22. Common mode transient immunity in the low state is the maximum tolerable  $dV_{CM}/dt$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (i.e.,  $V_0 < 1.0 \text{ V}$  or FAULT < 0.8 V).
- 23. To clamp the output voltage at  $V_{CC}$  3  $V_{BE}$ , a pull-down resistor between the output and  $V_{EE}$  is recommended to sink a static current of 650  $\mu$ A while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
- 24. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
- 25. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
- 26. Split resistors network with a ratio of 1:1 is needed at input LED1. See Figure 34.









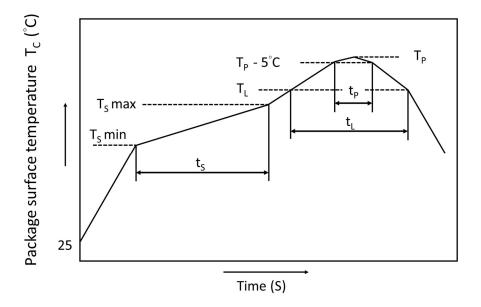




### PRECAUTIONS FOR SOLDERING

# **IR Reflow soldering**

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.



DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Preheat temperature	Ts	150	200	°C
Preheat time	ts	60	120	S
Ramp-up rate (T <sub>L</sub> to T <sub>P</sub> )			3	°C/s
Liquidus temperature	TL	2:	°C	
Time above T∟	t∟	60	100	S
Peak Temperature	T <sub>P</sub>		260	°C
Time during which T <sub>C</sub> is			20	
between (T <sub>P</sub> - 5) and T <sub>P</sub>	t₽		20	S
Ramp-down rate			6	°C/s