2.5 Amp Output Current IGBT Gate Driver Optocoupler

with Integrated (V_{CE}) Desaturation Detection, UVLO Fault Status Feedback, Active Miller Clamp and Auto-Fault Reset

Description

The SJS-333J is an advanced 2.5 A output current, easy-to-use, intelligent gate driver which makes IGBT V_{CE} fault protection compact, affordable, and easy-to implement. Features such as integrated V_{CE} detection, under voltage lockout (UVLO), "soft" IGBT turn-off, isolated open collector fault feedback and active Miller clamping provide maximum design flexibility and circuit protection.

The SJS-333J contains a LED. The LED is optically coupled to an integrated circuit with a power output stage. SJS-333J is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The voltage and current supplied by these optocouplers make them ideally suited for directly driving IGBTs with ratings up to 1200 V and 150 A.

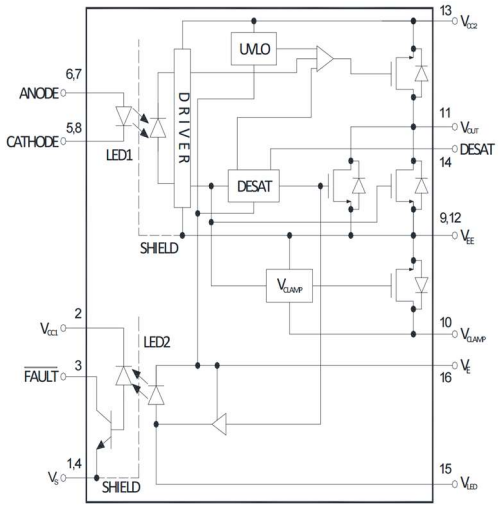
For IGBTs with higher ratings, the SJS-333J can be used to drive a discrete power stage which drives the IGBT gate.

The SJS-333J has an insulation voltage of V_{IORM} = 1414 V_{PEAK}.

Features

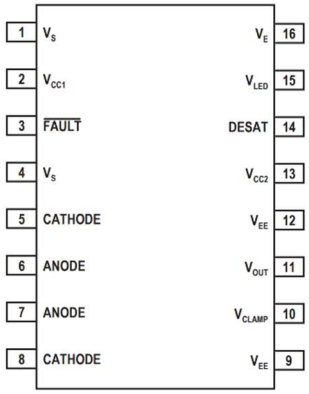
- *2.5 A maximum peak output current*
- *2.0 A minimum peak output current*
- *250 ns maximum propagation delay over temperature range*
- *1.7 A Active Miller Clamp. Clamp pin short to V_{EE} if not in used*
- *Miller Clamping*
- *Desaturation Detection*
- *Under Voltage Lock-Out Protection (UVLO) with Hysteresis*
- *"Soft" IGBT Turn-off*
- *Automatic Fault Reset after fixed Mute Time, typically 26 µs*
- *Available in SO-16 package*
- *100 ns maximum pulse width distortion (PWD)*
- *50 kV/µs minimum common mode rejection (CMR) at V_{CM} = 1500 V*
- *I_{CC} (max) < 5 mA maximum supply current*
- *Wide V_{CC} operating range: 15 V to 30 V over temperature range*
- *Wide operating temperature range: –40°C to 110°C*

Block Diagram



Applications

- *Isolated IGBT/Power MOSFET gate drive*
- *AC and brushless DC motor drives*
- *Industrial inverters and Uninterruptible Power Supply (UPS)*

SCHEMATIC	PIN DEFINITION
	1. V_S 16. V_E 2. V_{CC1} 15. V_{LED} 3. FAULT 14. DESAT 4. V_S 13. V_{CC2} 5. CATHODE 12. V_{EE} 6. ANODE 11. V_{OUT} 7. ANODE 10. V_{CLAMP} 8. CATHODE 9. V_{EE}

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	Note
Storage Temperature	Tstg	-55	125	°C	
Operating Temperature	T_A	-40	110	°C	2
Output IC Junction Temperature	T_J		125	°C	2
Average Forward Input Current	I_F		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	3
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	3
Positive Input Supply Voltage	V_{CC1}	-0.5	7.0	V	
FAULT Output Current	I_{FAULT}		8.0	mA	
FAULT Pin Voltage	V_{FAULT}	-0.5	V_{CC1}	V	
Total Output Supply Voltage	(V_{CC2} - V_{EE})	-0.5	35	V	
Negative Output Supply Voltage	(V_E - V_{EE})	-0.5	15	V	6
Positive Output Supply Voltage	(V_{CC2} - V_E)	-0.5	35-(V_E-V_{EE})	V	
Gate Drive Output Voltage	$V_{O(PEAK)}$	-0.5	V_{CC2}	V	
Peak Clamping Sinking Current	I_{Clamp}		1.7	A	
Miller Clamping Pin Voltage	V_{Clamp}	-0.5	V_{CC2}	V	
DESAT Voltage	V_{DESAT}	V_E	V_E+10	V	
Output IC Power Dissipation	P_O		600	mW	2
Input IC Power Dissipation	P_I		150	mW	2
Solder Reflow Temperature Profile	See Package Outline Drawings section				

RECOMMENDED OPERATION CONDITIONS					
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	Note
Operating Temperature	T_A	-40	110	°C	2
Total Output Supply Voltage	(V_{CC2} - V_{EE})	15	30	V	7
Negative Output Supply Voltage	(V_E - V_{EE})	0	15	V	4
Positive Output Supply Voltage	(V_{CC2} - V_E)	15	30-(V_E-V_{EE})	V	
Input Current (ON)	$I_{F(ON)}$	8	12	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V	

ELECTRICAL OPTICAL CHARACTERISTICS							
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note
INPUT CHARACTERISTICS							
FAULT Logic Low Output Voltage	V_{FAULTL}		0.01	0.4	V	I_{FAULT} = 1.1 mA, V_{CC1} = 5.5V	
			0.02	0.4	V	I_{FAULT} = 1.1 mA, V_{CC1} = 3.3V	
FAULT Logic High Output Current	I_{FAULTH}		0.01	0.5	µA	V_{FAULT} = 5.5 V, V_{CC1} = 5.5V	
			0.006	0.3	µA	V_{FAULT} = 3.3 V, V_{CC1} = 3.3V	
High Level Output Current	I_{OH}	-0.5	-2		A	V_O = V_{CC2} – 4	5
		-2.0			A	V_O = V_{CC2} – 15	3
Low Level Output Current	I_{OL}	0.5	2		A	V_O = V_{EE} + 2.5	5
		2.0			A	V_O = V_{EE} + 15	3
Low Level Output Current During Fault Condition	I_{OLF}	70	110	230	mA	V_{OUT} - V_{EE} = 14 V	6
High Level Output Voltage	V_{OH}	V_{CC}-0.5	V_{CC}-0.1		V	I_O = -650 µA	7,8,9,23
Low Level Output Voltage	V_{OL}		0.13	0.5	V	I_O = 100 mA	
Clamp Pin Threshold Voltage	V_{tClamp}		2.2		V		
Clamp Low Level Sinking Current	I_{CL}	0.35	1.0		A	V_O = V_{EE} + 2.5	
High Level Supply Current	I_{CC2H}		2.16	5	mA	I_O = 0 mA	9
Low Level Supply Current	I_{CC2L}		2.29	5	mA	I_O = 0 mA	
Blanking Capacitor Charging Current	I_{CHG}	0.13	-0.23	-0.33	mA	V_{DESAT} = 2 V	9,10
Blanking Capacitor Discharge Current	I_{DSCHG}	10	31		mA	V_{DESAT} = 7.0 V	
DESAT Threshold	V_{DESAT}	6	6.7	7.5	V	V_{CC2} -V_E >V_{UVLO-}	9
UVLO Threshold	V_{UVLO+}	10.5	11.5	12.5	V	V_O > 5 V	7,9,11
	V_{UVLO-}	9.2	10.5	11.1	V	V_O < 5 V	7,9,12
UVLO Hysteresis	(V_{UVLO+} - V_{UVLO-})	0.4	1		V		
Threshold Input Current Low to High	I_{FLH}		0.33	5	mA	I_O = 0 mA, V_O > 5 V	
Threshold Input Voltage High to Low	V_{FHL}	0.8	1.75		V		

Input Forward Voltage	V_F	1.6	2.0	2.4	V	I_F = 10 mA	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA	
Input Capacitance	C_{IN}		70		pF	f = 1 MHz, V_F = 0 V	

■ *Unless otherwise noted, all typical values at T_A = 25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V ; all Minimum/Maximum specifications are at Recommended Operating Conditions.*

SWITCHING SPECIFICATION							
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note
SWITCHING CHARACTERISTICS							
Propagation Delay Time to Output Low Level	t_{PHL}	50	114	250	ns	Rg = 10 Ω, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{CC2} = 30 V	
Propagation Delay Time to Output High Level	t_{PLH}	50	87	250	ns		13,15
Pulse Width Distortion	PWD	-100		100	ns		14,17
Propagation Delay Difference Between Any Two Parts	PDD (t_{PHL} - t_{PLH})	-150		150	ns		17,16
Rise Time	t_r		55		ns		
Fall Time	t_f		44		ns		
DESAT Sense to 90% VO Delay	$t_{DESAT(90\%)}$		0.1	0.5	µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	19
DESAT Sense to 10% VO Delay	$t_{DESAT(10\%)}$		2.2	3	µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ , Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	
DESAT Sense to Low Level FAULT Signal Delay	$t_{DESAT(FAULT)}$		0.2	0.5	µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, C_F = Open, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	18
			0.8		µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, C_F = 1 nF, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	
DESAT Sense to DESAT Low Propagation Delay	$t_{DESAT(LOW)}$		0.15		µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC2} = 30 V	19
DESAT Input Mute	$t_{DESAT(MUTE)}$	15	26	40	µs	C_{DESAT} = 100 pF, R_F = 2.1kΩ, Rg = 10 Ω, Cg = 10 nF, V_{CC1} = 5.5V, V_{CC2} = 30 V	20

Output High Level Common Mode Transient Immunity	$\|CM_H\|$	15			kV/μs	T_A = 25°C, I_F = 10 mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 15 pF	21
		50				T_A = 25°C, I_F = 10 mA V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 1 nF	21,26
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	15			kV/μs	T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 15 pF	22
		50				T_A = 25°C, V_F = 0 V V_{CM} = 1500 V, V_{CC2} = 30 V, R_F = 2.1 kΩ, C_F = 1 nF	

■ *Unless otherwise noted, all typical values at T_A = 25°C, V_{CC2} - V_{EE} = 30 V, V_E - V_{EE} = 0 V ; all Minimum/Maximum specifications are at Recommended Operating Conditions.*

ISOLATION CHARACTERISTIC								
PARAMETER	SYMBOL	DEVICE	MIN.	TYP.	MAX.	UNIT	TEST CONDITION	Note
Withstand Insulation Test Voltage	V_{ISO}	SJS-333J	5000	-	-	V	RH ≤ 40%-60%, t = 1min, T_A = 25 °C	24,25
Input-Output Resistance	R_{I-O}	-	-	10^{12}	-	Ω	V_{I-O} = 500V DC	25

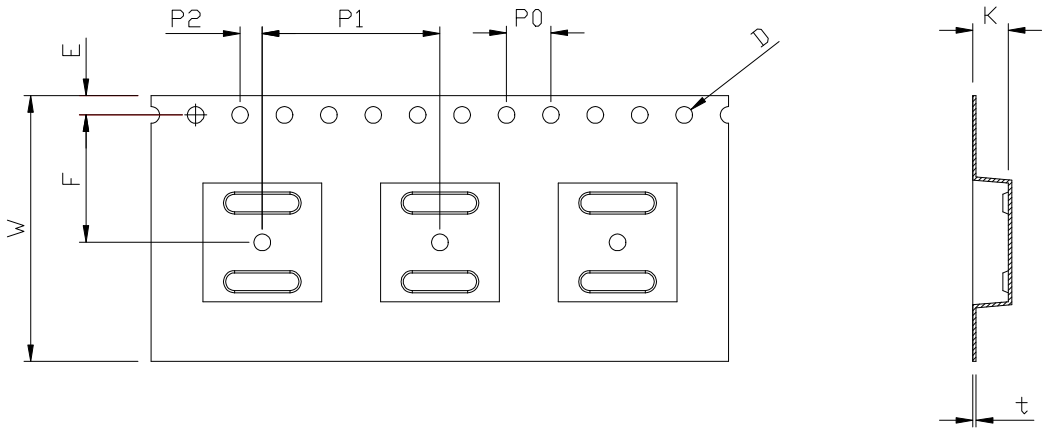
Notes:

1. Derate linearly above 70°C free air temperature at a rate of 0.3 mA/°C.
2. In order to achieve the absolute maximum power dissipation specified, pins 4, 9, and 10 require ground plane connections and may require airflow. See the Thermal Model section in the application notes at the end of this data sheet for details on how to estimate junction temperature and power dissipation. In most cases the absolute maximum output IC junction temperature is the limiting factor. The actual power dissipation achievable will depend on the application environment (PCB Layout, air flow, part placement, etc.). See the Recommended PCB Layout section in the application notes for layout considerations. Output IC power dissipation is derated linearly at 10 mW/°C above 90°C. Input IC power dissipation does not require derating.
3. Maximum pulse width = 10 μs. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0 A. Derate linearly from 3.0 A at +25°C to 2.5 A at +105°C. This compensates for increased I_{OPEAK} due to changes in V_{OL} over temperature.
4. This supply is optional. Required only when negative gate drive is implemented.
5. Maximum pulse width = 50 μs.
6. See the Slow IGBT Gate Discharge During Fault Condition section in the applications notes at the end of this data sheet for further details.

7. 15 V is the recommended minimum operating positive supply voltage (V_{CC2} - V_E) to ensure adequate margin in excess of the maximum V_{UVLO+} threshold of 12.5 V. For High Level Output Voltage testing, V_{OH} is measured with a dc load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.
8. Maximum pulse width = 1.0 ms.
9. Once VO of the SJS-333J is allowed to go high (V_{CC2} - V_E > V_{UVLO+}), the DESAT detection feature of the SJS-333J will be the primary source of IGBT protection. UVLO is needed to ensure DESAT is functional. Once V_{CC2} is increased from 0V to above V_{UVLO+}, DESAT will remain functional until V_{CC2} is decreased below V_{UVLO-}. Thus, the DESAT detection and UVLO features of the SJS-333J work in conjunction to ensure constant IGBT protection.
10. See the DESAT fault detection blanking time section in the applications notes at the end of this data sheet for further details.
11. This is the “increasing” (i.e. turn-on or “positive going” direction) of V_{CC2} – V_E
12. This is the “decreasing” (i.e. turn-off or “negative going” direction) of V_{CC2} – V_E
13. This load condition approximates the gate load of a 1200 V/150A IGBT.
14. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given unit.
15. As measured from I_F to V_O.
16. The difference between t_{PHL} and t_{PLH} between any two SJS-333J parts under the same test conditions.
17. As measured from ANODE, CATHODE of LED to V_{OUT}
18. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.
19. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.
20. Auto Reset: This is the amount of time when V_{OUT} will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.
21. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V or FAULT > 2 V).
22. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V or FAULT < 0.8 V).
23. To clamp the output voltage at V_{CC} - 3 V_{BE}, a pull-down resistor between the output and V_{EE} is recommended to sink a static current of 650 µA while the output is high. See the Output Pull-Down Resistor section in the application notes at the end of this data sheet if an output pull-down resistor is not used.
24. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in IEC/EN/DIN EN 60747-5-5 Insulation Characteristic Table.
25. This is a two-terminal measurement: pins 1-8 are shorted together and pins 9-16 are shorted together.
26. Split resistors network with a ratio of 1:1 is needed at input LED1. See Figure 31.

TAPING DIMENSIONS (Dimensions in mm unless otherwise stated)

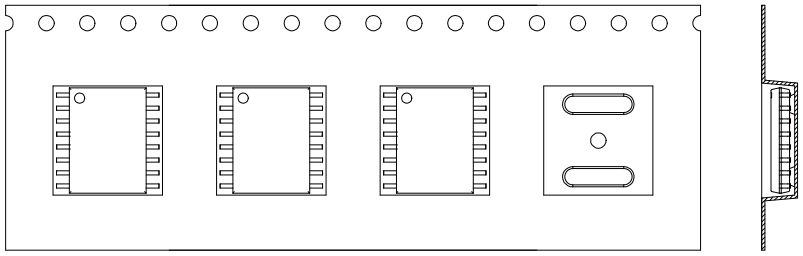
Taping Dimensions



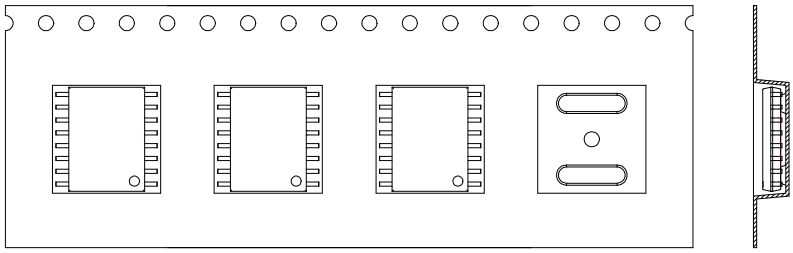
Dimension Symbol	D	E	F	P0	P1	P2	t	W	K
Dimension (mm)	1.5±0.1	1.75±0.1	11.5±0.1	4.0±0.1	16.0±0.1	2.0±0.1	0.3±0.1	24.0±0.3	3.2±0.1

Tape & Reel Packing Specifications

Option T1

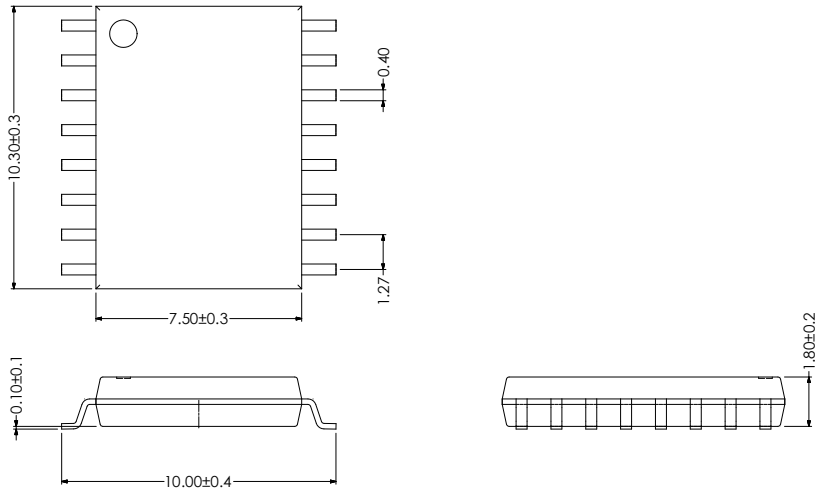


Option T2

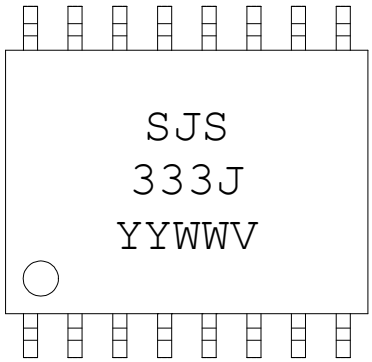


PACKAGE DIMENSIONS (Dimensions in mm unless otherwise stated)

SURFACE MOUNT LEAD FORMING



MARKING AND ORDERING INFORMATION



MARKING SYMBOL	DESCRIPTION
SJS	Part Number
333J	
YY	Year Date Code
WW	Two Digit Work Week
V	VDE Option (V or None)

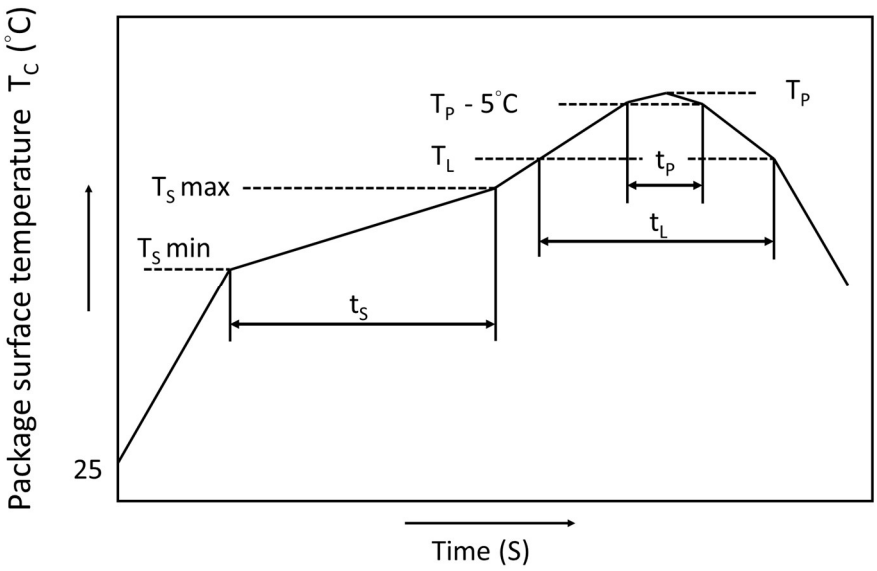
S	J	S	–	3	3	3	J	–	T1	V

Part Number — Option T1/T2 — VDE option

PRECAUTIONS FOR SOLDERING

IR Reflow soldering

One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.



DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Preheat temperature	T_S	150	200	°C
Preheat time	t_S	60	120	s
Ramp-up rate (T_L to T_P)			3	°C/s
Liquidus temperature	T_L	217		°C
Time above T_L	t_L	60	100	s
Peak Temperature	T_P		260	°C
Time during which T_C is between (T_P - 5) and T_P	t_P		20	s
Ramp-down rate			6	°C/s